Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Y1**
2. **Y2**
3. **–VS**
4. **W2**
5. **W1**
6. **+VS**
7. **X1**
8. **X2**

**1**

**2**

**3**

**4 5**

**8**

**7**

**6**

**.054”**

**.054”**

**AD834PMD**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Au or Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: AD834PMD**

**APPROVED BY: DK DIE SIZE .054” X .054” DATE: 5/31/16**

**MFG: ANALOG DEVICES THICKNESS .023” P/N: AD834**

**DG 10.1.2**

#### Rev B, 7/1